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14. ABSTRACT
The primary goal of this research was to investigate DSP hardware techniques to support the sharing of transmit hardware and array apertures between multiple simultaneous users of Navy RF Systems, specifically with respect to the implementation of delta-sigma converter based DSP systems. In particular, we considered (1) tradeoffs between speed, space and power (2) finite precision analysis techniques to effect efficient hardware designs, and (3) algorithm and hardware considerations for critical path minimization. Specific investigations of candidate DSP architectures, including implementations in Xilinx FPGAs, allowed us to evaluate the performance of several alternate approaches.

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Final Report

Efficient DSP Hardware Implementations for Navy RF Systems

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Research Objective

The primary goal of this research was to investigate DSP hardware techniques to support the sharing of transmit hardware and array apertures between multiple simultaneous users of Navy RF Systems, specifically with respect to the implementation of delta-sigma converter based DSP systems. In particular, we considered (1) tradeoffs between speed, space and power (2) finite precision analysis techniques to effect efficient hardware designs, and (3) algorithm and hardware considerations for critical path minimization. Specific investigations of candidate DSP architectures, including implementations in Xilinx FPGAs, allowed us to evaluate the performance of several alternate approaches.

Reduced Scope

The IRST/Radar program under which this work was funded was discontinued. No FY2009 funds were provided to support the grant. Consequently, the scope of our work was reduced. The original grant was for $300,000 over 3 years. The current funding level is $189, 274. We were compelled to eliminate all third year tasks from the original proposal due to lack of funding.

Task 1: Develop and analyze candidate system architectures that balance speed, space, and power

This task was expected to require approximately 30% of the effort for the proposed project over the original three-year period. Consequently the candidate system architectures considered were significantly limited.

Task 2: Apply finite precision analysis techniques to the delta-sigma system

This task was expected to require approximately 30% of the effort for the proposed project over the original three year period. The principal results from this work were obtained in the first year of the proposed project, but we had limited time to apply these results to the delta-sigma system.

Task 3: Use algorithm and hardware innovations to minimize the critical path in the delta-sigma system

This task was expected to require approximately 40% of the effort for the proposed project. The task was originally planned to be addressed in the second and third years of the project. This task was significantly curtailed due to lack of funding.

Background and Motivation

Sharing of transmit hardware and array apertures between multiple simultaneous users of future Navy RF systems would in principle permit tremendous system flexibility, but inter-modulation distortion (IMD) products created in transmitter amplifiers have long been assumed to preclude this possibility. Such spectral-purity issues are not confined to future systems: in key areas of the world today some fleet radars are not allowed to radiate; they cannot be used at all. The best long-term prospect for robustly solving both problems lies in replacing the high power amplifier (HPA) in the Transmit-Receive

module with direct digital waveform synthesis at higher power levels, thus removing the need for that amplifier. The only synthesis approach on the horizon that can offer suitably low IMD and spurious levels appears to be noise-shaping D/A conversion, in which a digital delta-sigma modulator drives an RF power circuit realizing linear pulse modulation. Unfortunately, real-time delta-sigma modulators do not exist at the required microwave sample rates, nor are they likely to be forthcoming from industry.

Conventional Nyquist-rate D/A converters, which attempt to spread quantization noise evenly across the frequency band, are generally limited by nonlinearities in the quantizer to about 14-16 bits of resolution without the use of expensive and tedious trimming and matching techniques [0-3]. Noise-shaped conversion [4-6] uses a much higher data rate than the bandwidth of the signal to be converted, along with a low-resolution (often one bit) quantizer to achieve high in-band linearity. This is accomplished by embedding the quantizer in a feedback loop designed to spectrally shape the quantization noise and effectively push that noise out of the signal frequency band. The highly quantized output is then converted to analog via linear pulse modulation, and the out-of-band quantization noise is removed with a bandpass filter. The price of this high resolution is not just the higher data rate (which is partially offset by the simpler quantizer), but also the risk of somewhat unpredictable instabilities not present in conventional converters. The hardware clock rates required can be reduced using parallelization techniques developed at NRL[7-8] and by using multilevel quantizer implementations[9]. The latter also improves stability but leads to inevitable hardware-mismatch errors. Techniques developed at NRL [5,6,8] and elsewhere [10-14] use a dynamic quantizer implementation to spectrally shape mismatch errors out of the signal band much in the way that the delta-sigma modulator shapes quantization errors. Many aspects of the structure of parallel and multilevel quantizer architectures are also incorporated in the basic delta-sigma modulator, and so implementation techniques applicable to one generally apply to all.

To implement such a system using FPGA (or ASIC) hardware approaches requires a thorough understanding of the algorithms involved, as well as the use of innovative computer arithmetic and digital hardware design techniques. We have a great deal of experience in the hardware implementation of DSP systems, especially concerning the inevitable tradeoff of speed, space, and power. We have previously worked with the NRL on variable bit-precision implementation of digital filters [15-16], which is also applicable here.

Approach

Even though we had a significant reduction in funding, we made significant progress on the interrelated tasks that comprise this work:

Task 1: Develop and analyze candidate system architectures that balance speed, space, and power

In complex VLSI designs, including FPGAs and ASICs, there is always a fundamental balance between the maximum speed at which the circuit can be operated, the amount of chip area consumed by the circuit, and the power consumed by the operating circuit. In the proposed delta-sigma implementation, the circuit area will be dominated by the loop

filter [5,7]. Our previously developed approaches, e.g. [17,20], as well as those of other researchers, was applied to this particular problem. A naïve implementation approach was explored to estimate hardware requirements for the system. The nature of the delta-sigma system requires novel applications of known techniques since the filter is itself embedded in a feedback loop which poses some additional challenges to the analysis and design. We have developed VHDL designs for the loop filter implementation based on different candidate architectures, as well as a VHDL design of a simple delta-sigma converter that will be the basis of integrating our designs in this project. We also explored new designs, particularly for high performance implementations of the loop filter based on multiple constant multiplication (MCM).

Task 2: Apply finite precision analysis techniques to the delta-sigma system
Theoretical analysis of digital signal processing algorithms, including delta-sigma approaches, routinely uses double-precision floating point number representations for simplicity. Although some Matlab™ tools do include limited capability for considering finite precision effects, detailed analysis requires custom simulations. This high level of analysis is required to understand the finite precision effects so that they can be used to create better implementations. Specifically, our previous research [**Error! Reference source not found.**,19,20,21] has shown that using variable levels of precision can result in a better tradeoff between performance and space – not all bits have equal importance to the design. We can use our analysis to develop design techniques that create more practically realizable implementations. Finite precision effects were considered for new hardware implementations. We considered the effects of finite precision effects in terms of the coefficient quantization and the internal rounding for MCM implementations and designed approaches for implementing significantly smaller circuits through the use of carefully designed quantization algorithms.

Task 3: Use algorithm and hardware innovations to minimize the critical path in the delta-sigma system
The nature of the delta-sigma problem yields a unique opportunity to manage the critical path for maximum throughput. The feedback loop complicates the analysis and implementation of the delta-sigma system. Although the critical path does include the feedback loop, the inherent timing constraints in the delta-sigma converter still allows us to implement the FIR loop filter using high-throughput pipeline implementation techniques. Thus, we can calculate some results quite early, which can be used to effectively reduce the critical path.

Long Term Proposed Research

We have begun preliminary investigations into the design of sparse filters using 1-norm criteria. Using results from Donoho used in denoising, we should also be able to develop efficient techniques for designing sparse filters using entropy-based criteria. One possibility is through direct minimization of entropy instead of energy. Probably more fruitful would be approaches based on the Hirschman Uncertainty, such as an approach that uses the Hirschman Optimal Transform (HOT) developed by V. DeBrunner along with T. Przebinda and M. Ozaydin[22]. Further improvements can be achieved by combining these approaches with design optimizations for sparseness, such as that proposed by O. Gustafsson, L.

DeBrunner, V. DeBrunner, and H. Johansson[23]. By combining these sparse designs with multiple constant multipliers (MCM) and computer arithmetic techniques based on number representation, hardware implementations of filters for a wide range of high performance applications are possible. The developed designs would be of great use in fixed implementations of fast mixed signal and DSP systems, but also in the application of adaptive filters in communications and electronic sensing (both passive and active).

Summary of Key Results

In the first year of the project, we developed a Multiple Constant Multiplier (MCM) design that can operate at approximately 320 MHz and uses less area that more traditional design approaches. Analysis of coefficient quantization effects indicates that a large number of bits are required for coefficients to achieve acceptable performance.

In the second year of the project we focused on the implementation of the delta-sigma loop filter. We have studied the impact of sparse coefficients and the use of multiple constant multiplier (MCM) techniques to reduce the hardware requirements of the filter. In addition, we have investigated the effects that embedded hardware blocks, such as the Xilinx DSP48 slice, have on FPGA filter designs optimized using MCM techniques.

Related Publications

Three Masters in Electrical & Computer Engineering completed work directly related to this research project:

- Abhijit Patil, *FPGA Implementation of Digital Filters Using MCM,* MS EE thesis, Florida State University, 2009.
- Sean Patronis, *Sparse FIR Filters and The Impact on FPGA Area Usage,* MS EE thesis, Florida State University, 2008.
- Charles Howard, *Minimizing FIR Filter Designs Implemented in FPGAs Utilizing Minimized Adder Graph Techniques,* MS EE thesis, Florida State University, 2008.

The accomplishments of this research and related work are demonstrated in several international publications. These publications give additional details of the completed work.

- Rui Guo, Linda S. DeBrunner, and Kenny Johansson, "Truncated MCM Using Pattern Modification for FIR Filter Implementation," *Proc. IEEE International Symposium on Circuits and Systems (ISCAS),* Paris, France, 2010.
- K. Johansson, O. Gustafsson, L. S. DeBrunner, "Estimation of the switching activity in shift-and-add based computations," *Proc. IEEE International Symposium on Circuits and Systems (ISCAS),* Taipei, Taiwan, pp. 3055-3057, 2009.
- Rui Guo, Lei Wang, and Linda DeBrunner, "A Novel FIR Filter Implementation Using Truncated MCM Technique," *Proc. Asilomar Conference on Signals, Systems, and Computers,* Pacific Grove, California, 2009.
- Kenny Johansson, Linda DeBrunner, Oscar Gustafsson, and Victor DeBrunner, "Design of Multiplierless FIR Filters with an Adder Depth Versus Filter Order Trade-Off," *Proc. Asilomar Conference on Signals, Systems, and Computers.* Pacific Grove, California, 2009.

- Charles D. Howard and Linda S. DeBrunner, "High speed DSP block for FPGA devices using a programmable adder graph," *Proc. IEEE 13th Digital Signal Processing Workshop and 5th IEEE Signal Processing Education Workshop, DSP/SPE 2009*, Marco Island, Florida, pp. 490-494, 2009.
- Sean Patronis and Linda DeBrunner, "Sparse FIR Filters and their Impact on FPGA Area Usage," *Proc. Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove California, pp. 1862- 1866, 2008.
- Charles D. Howard, Linda S. DeBrunner, and Victor DeBrunner, "Hybrid Multiple Constant Multiplication Implementation for FIR Filters in FPGA Devices," *Proc. Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, California, pp. 1422-1425, 2007.
- Linda S. DeBrunner, "Reducing Complexity of FIR Filter Implementations for Low Power Applications," *Proc. Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, California, pp. 1407-1411, 2007.
- Oscar Gustafsson, Linda S. DeBrunner, Victor DeBrunner, and Håkan Johansson, "On the Design of Sparse Half-Band Like FIR Filters," *Proc. Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, California, pp. 1098-1102, 2007.

References

1. L. R. Carley, "A noise-shaping coder topology for 15+ bit converters," *IEEE Journal of Solid-State Electronics,* vol. 24, issue 2, pp. 267-273, April 1989.
2. B. A. Wooley, "Cascaded noise-shaping modulators for oversampled data conversion,"*Proc. IEEE Custom Integrated Circuits Conf.,* pp. 113-114, September 2003.
3. I. Galton, "Noise-shaping D/A converters for $\Delta\Sigma$ modulation," *ISCAS,* vol. 1, pp. 441-444, May 1996.
4. I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," *IEEE Trans. Circuits and Systems II,* vol. 44, no. 10, pp. 808-817, October 1997.
5. D. P. Scholnik and J. O. Coleman, "Joint shaping of quantization and hardware-mismatch errors in a multibit delta-sigma DAC," *Proc. Midwest Symp. On Circuits and Systems (MWSCAS 2000),* Lansing, MI, August *2000.*
6. D. P. Scholnik, J. O. Coleman, D. Bowling, and M. Neel, "Spatio-temporal delta-sigma modulation for shared wideband transmit arrays," *Proc. IEEE Radar Conf.,* pp. 85-90, April 2004.
7. Dan P. Scholnik, "A parallel digital architecture for delta-sigma modulation," *IEEE Int'l Midwest Symp. on Circuits and Systems (MWSCAS 2002),* pp. 352-355, August 2002
8. D. P. Scholnik and J. O. Coleman, "Space-time vector delta-sigma modulation," *ISCAS 2002,* vol. 3, pp. 719-722, 2002.
9. V. Sharma, Un-Ku Moon, and G. C. Temes, "A Generic Multi-level Multiplying D/A converter for Pipelined ADCs," *ISCAS,* pp. 6182-6185, May 2005.
10. Bingxin Li and H. Tenhunen, "A second order sigma delta modulators using semi-uniform quantizer with 81dB dynamic range at 32x OSR," *Proc. European Solid-State Circuits Conf.,* pp. 579-582, Sept. 2002.
11. G. Einarsson, "Dynamic range and error dissipation of adaptive quantizers," *IEEE Trans on Acoustics, Speech, and Signal Processing,* vol. 33, issue 5, pp. 1073-1075, Oct. 1985.
12. C. Xydeas, M. Faruqui, and R. Steele, "Envelope Dynamic Ratio Quantizer," *IEEE Trans. Communications,* vol. 28, issue 5, pp. 720-728, May 1980.
13. A. V. Trushkin, "On the design of an optimal quantizer," *IEEE Tran. Information Theory,* vol. 39, issue 4, pp. 1180-1194, July 1993.
14. Mr. R. Miller and C. S. Petrie, "A multibit sigma-delta ADC for multimode receivers," *IEEE Tran. Solid-State Circuits,*
15. L. S. DeBrunner, V. E. DeBrunner, and D. Bhogaraju, "Defining canonical-signed-digit number systems as arithmetic codes," *Proc. Asilomar Conf. Signals, Systems, and Computers,* vol. 2, pp. 1593-1597, Nov. 3-6, 2002.
16. L. S. DeBrunner, V. E. DeBrunner, and D. Bhogaraju, "Using variable length 13-ary, radix-4 CSD coefficients to achieve low-area implementations of FIR filters," *Proc. Midwest International Symposium on Circuits and Systems (MWSCAS),* vol. 3, pp. 5-8, Aug. 4-7, 2002.
17. V. E. DeBrunner, L. S. DeBrunner, S. Coone, and X.-J. Hu, "Using Entropy to Build Efficient FIR Digital Filters," *Proc. of the IEEE DSP Workshop,* Taos Ski Valley, New Mexico, August 2004.

18. V. DeBrunner, L. DeBrunner, and Longji Wang, "Combined sub-band and frequency domain adaptive algorithm for active control," *Proc. Digital Signal Processing Workshop and Signal Processing Education Workshop,* pp. 211-216, Oct. 13-16, 2002.
19. Victor DeBrunner, Linda DeBrunner, and Anand Mohan, "Using 2nd-Order Information to Reduce Average Coefficient Length in IIR Filters," *ISCAS 2002,* Phoenix, Arizona, pp. 189-192, 2002.
20. Xiaojuan Hu, Linda DeBrunner, and Victor DeBrunner, "An Efficient Design for FIR Filters with Variable Precision," *ISCAS 2002,* Phoenix, Arizona, pp. 365-368, 2002.
21. Linda S. DeBrunner, Victor DeBrunner, Xiaojuan Hu, Olivier Demuynck and Andi Swartztrauber, "A reduced-space half-band filter design on an Actel FPGA," *35th Annual Asilomar Conference on Signals, Systems, and Computers,* Pacific Grove, California, pp. 1237-1240, November 2001.
22. T. Przebinda, V. DeBrunner, and M. Özaydin, "The optimal transform for the discrete Hirschman uncertainty principle," *IEEE Transactions on Information Theory,* vol 47, issue 5, pp. 2086-2090, July 2001.
23. Oscar Gustafsson, Linda S. DeBrunner, Victor DeBrunner, and Håkan Johansson, "On the Design of Sparse Half-Band Like FIR Filters," *Proc. Asilomar Conference on Signals, Systems, and Computers,* pp. 1098-1102, 2007.